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Patent No. : 7,187,038 B2  
Inventor(s) : Pierre Morin, et al.  
Issued : March 6, 2007  
For SEMICONDUCTOR DEVICE WITH  
MOS TRANSISTORS WITH AN ETCH-STOP  
LAYER HAVING AN IMPROVED RESIDUAL  
STRESS LEVEL AND METHOD FOR  
FABRICATING SUCH A SEMICONDUCTOR  
DEVICE

Doc. No. 02GR109854488

To Whom It May Concern:

The Certificate of Correction issued on August 7, 2007, issued in error, in that error(s) was made in identifying the patent number and/or keying text/corrections, i.e.:

The issue date in the heading of cofc has been incorrectly entered in the heading of the issued cofc. A superseding cofc will be issued to correct the patent issue date to read --March 6, 2007--

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Therefore, a certificate of correction will be issued to correct (supersede) the Certificate of Correction containing error(s), made during preparation of the Certificate of Correction, as noted above.

No further response is required, from applicants (attorney). However, errors discovered by attorney, other than as noted and described above, should be noted on *a copy* of the Certificate of Correction that was issued in error, accompanied by a signed transmittal letter and submitted directed to this Branch.

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cbn